# Design Verification Internship

Design your first work experience with us!

**Who can apply:**

- Students in the third or fourth year of their B. Sc. degree and M. Sc. degree students in Electronics, Informatics, Computer Science, Automatic, Telecommunications or Electrical engineering.

**Project:**

- Verification of a protocol converter module

**Description:**

- The candidate will verify functional correctness of a bus splitter module using UVM methodology and SystemVerilog language.
- In the first stage, UVCs (Universal Verification Components) for interfaces/protocols used by the protocol converter module will be created, and in the second stage, a complete UVM environment for verification of the module will be written, and a randomized test regression for its verification will be run.
- The project will be implemented using Cadence tool suite.

**Prerequisites**

- At least B level of English language (spoken and written)

**Why to choose to work for HDL Design House:**

- Paid internship
- No lock-in contract obligation
- Working in young and enthusiastic team
- Opportunity to work on projects for some of the best Semiconductor companies in the world

**Application deadline:**

- 21st of March