Evaluation and analysis of an on-line error detection monitoring technique

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References:

Abstract:
A previously proposed technique for on-line monitoring of program control flow is extensively evaluated in the paper. This technique, which employs an external monitor, is briefly described. The performance evaluation was carried out in a specially designed simulation environment that can inject artificial faults according to the single bit-flip model. The faults were injected in the processor itself, on the bus lines and in the memory. An evaluation study was conducted with a representative benchmark program. First, the memory overhead and execution time overhead of the monitored program were obtained. Then, typical performance indicators such as error detection and latency were presented for the different fault categories itemized by the location and means of detection. The results thoroughly discussed in this paper show that the technique is able to detect a high percentage of the injected faults manifested as control flow errors with an acceptable time and memory overhead.

Keywords:
hardware monitor, simulation analysis, fault injection, fault tolerance, control flow graph, on-line monitoring technique