Sources of Parallelism in Software Pipelining Loops with Conditional Branches

D. Milićev, Z. Jovanović

References:

ACM SIGPLAN NOTICES, Vol. 35, No. 2, pp. 36-45, Feb, 2000

Abstract:

The subject of this paper is the instruction-level parallelism and the process of software pipelining loops with conditional branches. First, preconditions for treating such loops are introduced, and some effects of existence of conditional instructions and their outcomes that are important for parallelization are analyzed. These effects are emphasized and systematized.

Keywords:

loops with conditional branches, instruction-level parallelism, software pipelining